UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,451	06/20/2001	Thomas L. Ritzdorf	291958170US02	3390

25096 7590 01/12/2006

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
LEADER, WILLIAM T	
ART UNIT	**PAPER NUMBER**
1742	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,451	RITZDORF ET AL.	
	Examiner	Art Unit	
	William T. Leader	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *68-78,80-85 and 107-116* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *68-78,80-85 and 107-116* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt of the papers filed o October 137, 2005, is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 68-78 and 80-84 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 68 recites the limitation "microelectronic workpiece" in lines 3 and 15. There is insufficient antecedent basis for this limitation in the claim. "Microelectronic" has been changed to "semiconductor" in line 2. In independent claims 80, 82 and 84 include the expression "the microelectronic workpiece" but have been amended to recite a "semiconductor" in the preamble. Claim 85 similarly recites a microelectronic workpiece in line 11.

Claim Rejections - 35 USC § 103

5. Claims 68-78, 80-85 and 107-115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) combined with the Lowenheim text *Electroplating* and the Alkire article "Transient behavior during electrodeposition onto a metal strip of high ohmic resistance", in view of Ameen et al (US 5,685,970) and Ohmura et al (4,401,521) and further in

view of Venkatraman et al (5,814,557) and Merchant et al (5,863,666) for the reasons given in the previous office action and in view of the following comments.

6. Claim 116 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) combined with the Lowenheim text *Electroplating* and the Alkire article "Transient behavior during electrodeposition onto a metal strip of high ohmic resistance", in view of Ameen et al (US 5,685,970) and Ohmura et al (4,401,521) and further in view of Venkatraman et al (5,814,557) and Merchant et al (5,863,666) as applied to claims 68-78, 80-85 and 107-115 above, and further in view of Bernhardt et al (5,256,565) for the reasons given in the previous office action and in view of the following comments.

7. Applicant's Remarks have been carefully considered but are not deemed to be persuasive. With respect to Venkatraman et al applicant argues that the annealing step first that the annealing step is optional and second that the step drives copper from the second deposited layer into the first deposited layer. This argument is not convincing. With respect to the annealing step being optional, Venkatraman et al teach that the anneal step may be omitted if the temperatures of subsequent processing to a semiconductor device are sufficient to drive the copper into the first conductive layer (column 3, lines49-52). This suggests that heating during subsequent processing is equivalent to a separate annealing step. Additionally, Venkatraman et al teach that 'some" of the copper is diffused into the first layer. Thus, a discrete layer of copper remains.

8. It is noted that Poris et al note that if a void forms during plating of a contact, it would be filled with electrolyte which could lead to reliability problems due to corrosion or explosion upon heating due to the conversion of a liquid to a gas (column 4, lines 56-59). Since the electrolyte used to electrolytically deposit the copper onto the semiconductor workpiece is an aqueous solution (column 12, line 13), conversion of the electrolyte to a gas would be expected to occur at a temperature of approximately 100°C. This temperature falls within the range of "less than about 250°C recited in claims 71 and 109. Thus, Poris et al envision that subsequent to copper electroplating the workpiece may be subjected to elevated temperatures of about 100°C or more. As suggested by Venkatraman et al, such subsequent heating is equivalent to an annealing step.

9. With respect to Merchant, applicant argues that there is no suggestion to apply the annealing step to a semiconductor. Merchant teaches that the physical properties of copper are improved upon annealing. The improvement would occur regardless of the substrate on which the copper is deposited.

10. Claims 68-78 and 80-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) combined with the Lowenheim text *Electroplating* and the Alkire article "Transient behavior during electrodeposition onto a metal strip of high ohmic resistance", in view of Ameen et al (US 5,685,970) and Ohmura et al (4,401,521) and further in view of Ding et al (6,066,892).

11. Poris, Lowenheim, Alkire, Ameen et al and Ohmura et al are interpreted and applied as above. Applicant has amended independent claims 68, 80, 82 and 84 to recite a semiconductor workpiece. As noted above, applicant argues that there is no suggestion for applying the annealing process taught in Merchant to semiconductor workpieces. Claims 68, 80, 82 and 84 have been amended to recite a semiconductor workpiece.

12. The Ding et al patent is directed to the use of copper metallization in the formation of an integrated circuit. After a copper alloy seed layer is deposited, a via hole is filled by a second deposition step with relatively pure copper. The full-fill deposition may be performed by a number of techniques including electroplating (column 5, lines 59-66). Ding et al observe that the copper seed layer oxidizes to form a surface layer of copper oxide (column 6, lines 406). Electroplating will naturally remove the copper oxide (column 6, line 13). When the fill copper is deposited by electroplating into the via, reflow temperatures of no more than 100°C are adequate (column 6, lines 17-20).

13. It would have been obvious to have annealed the semiconductor workpiece of Poris after electrolytic deposition of copper as taught by Ding et al because the copper deposit would have been improved.

14. Claims 68-78 and 80-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al (6,066,892 combined with the Lowenheim text *Electroplating* and the Alkire article "Transient behavior during electrodeposition onto a metal strip of high ohmic resistance", in view of Ameen et al (US 5,685,970) and Ohmura et al (4,401,521).

15. Ding et al, Poris, Lowenheim, Alkire, Ameen et al and Ohmura et al are interpreted and applied as above. It would have been obvious to have performed the copper electroplating step of Ding to fill the surface features by beginning at a low current density and increasing the current density after a period of time in which the thickness and current-carrying capacity of the plated layer had grown as taught by Lowenheim, Alkire, Ameen et al and Ohmura et al because a number of advantages resulting from the initial use of a low current density, including avoidance of burning the thin seed layer and increased uniformity of deposit, would have been obtained, and the advantage of shorter total deposition time and increased productivity would have been obtained by subsequently raising the current density. As noted above Ding et al teaches that the deposited copper layer may be reflowed at a temperature which need not be more than 100°C. This step corresponds to the elevated annealing step recited by applicant.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WL

William Leader
January 3, 2006

ROY KING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700